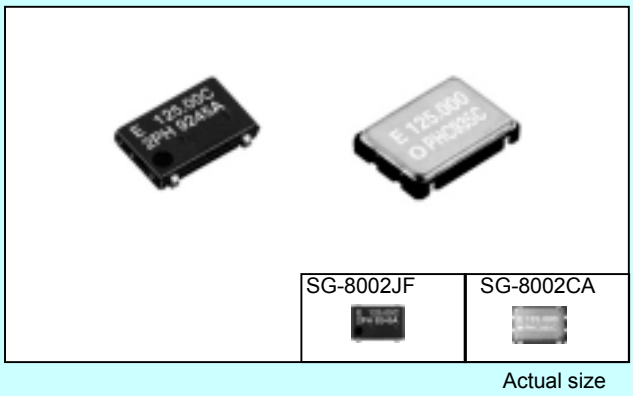
PROGRAMMABLE HIGH-FREQUENCY CRYSTAL OSCILLATOR

SG-8002JF / CA series

Product number (please contact us)

SG-8002JF : Q3308JFx1xxxx00
SG-8002CA : Q3309CAx0xxxx00

- Frequency range : 1 MHz to 125 MHz
- Operating voltage : 3.3 V or 5.0 V
- Function : Output enable(OE) or Standby(/ST)
- Thickness : 1.5 mm Max.
- Lead(Pb)-free : Complies with EU RoHS directive (Lead free completely:SG-8002CA)
- Pin compatible with ceramic package crystal oscillator (7 x 5):SG-8002JF
- Short lead mass production time by PLL technology.



Actual size

■ Specifications (characteristics)

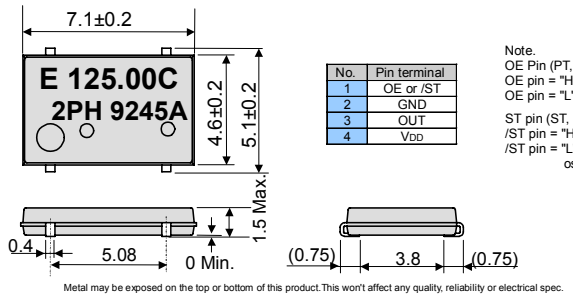
Item	Symbol	Specifications *2 PT / ST	PH / SH	PC / SC	Remarks
Output frequency range	f_0	1 MHz to 125 MHz		—	V_{DD}=4.5 V to 5.5 V
		—		1 MHz to 125 MHz	V_{DD}=3.0 V to 3.6 V
		—		1 MHz to 66.7 MHz	V_{DD}=2.7 V to 3.6 V
Operating voltage	V_{DD}	4.5 V to 5.5 V		2.7 V to 3.6 V	
Temperature range: Storage temperature	T_{STG}	-55 °C to +125 °C (CA:-40 °C to +125 °C)			Stored as bare product after unpacking
Temperature range: Operating temperature	T_{OPR}	-20 °C to +70 °C (-40 °C to +85 °C)		-40 °C to +85 °C	Refer to Application guide. "Frequency range"
Frequency stability	$\Delta f/f_0$	B: ±50 × 10^{-6} ,C: ±100 × 10^{-6}			B,C:-20 °C to +70 °C
		M: ±100 × 10^{-6}			M:-40 °C to +85 °C
Current consumption	I_{OP}	45 mA Max.		28 mA Max.	No load condition, Max. frequency range
Output disable current	I_{OE}	30 mA Max.		16 mA Max.	OE=GND(PT,PH,PC)
Standby current	I_{ST}	50 µA Max.			/ST=GND(ST,SH,SC)
Duty *1	tw/t	—	40 % to 60 %		CMOS load:50 % V_{DD}, Max. load condition
		40 % to 60 %	—		TTL load: 1.4V, Max. load condition
High output voltage	V_{OH}	V_{DD}-0.4 V Min.			I_{OH}=-16 mA(PT / ST,PH / SH),-8 mA(PC / SC)
Low output voltage	V_{OL}	0.4 V Max.			I_{OL}=16 mA(PT / ST,PH / SH), 8 mA(PC / SC)
Output loadcondition (TTL) *1	N	5TTL Max.	—		Max. frequency and Max. operating voltage
Output loadcondition (CMOS) *1	C_L	15 pF Max.			
Output enable / disable input voltage	V_{IH}	2.0 V Min.		70 % V_{DD} Min.	/ST, OE terminal
	V_{IL}	0.8 V Max.		20 % V_{DD} Max.	/ST, OE terminal
Output rise fall time *1	t_R / t_F	—	3 ns Max.		CMOS load: 20 % V_{DD} to 80 % V_{DD} level
		4 ns Max.	—		TTL load: 0.4 V to 2.4 V level
Oscillation start up time	t_{OSC}	10 ms Max.			Time at minimum operating voltage to be 0 s
Aging	fa	±5 × 10^{-6} / year Max.			T_a=+25 °C,V_{DD}=5.0 V/ 3.3 V (PC / SC) First year

*1 Operating temperature (-40 °C to +85 °C), the available frequency, duty and output load conditions, please refer to Page 40.
*2 PLL-PLL connection & Jitter specification, please refer to Page 41.
Checking possible by the Frequency Checking Program.

http://www.epsondevice.com/domcfg.nsf

■ External dimensions (Unit:mm)

● **SG-8002JF**



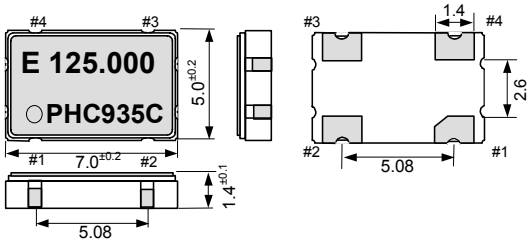
No.	Pin terminal
1	OE or /ST
2	GND
3	OUT
4	V_{DD}

Note.
OE Pin (PT, PH, PC)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

ST pin (ST, SH, SC)
/ST pin = "H" or "open" : Specified frequency output.
/ST pin = "L" : Output is low level (weak pull - down), oscillation stops.

Metal may be exposed on the top or bottom of this product.This won't affect any quality, reliability or electrical spec.

● **SG-8002CA**



No.	Pin terminal
1	OE or /ST
2	GND
3	OUT
4	V_{DD}

■ Recommended soldering pattern (Unit:mm)